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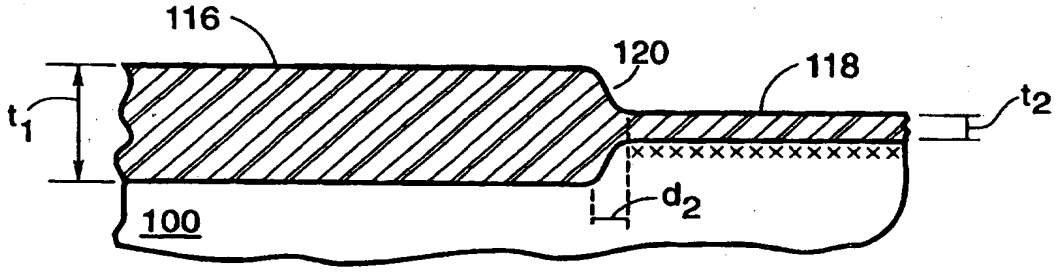
(54) Title: REDUCED BIRD'S BEAK FIELD OXIDATION PROCESS USING NITROGEN IMPLANTED INTO ACTIVE REGION



(57) Abstract

A method of forming a self-aligned filed oxide isolation structure without using silicon nitride. The method comprises forming a dielectric on an upper surface of a semiconductor substrate. The upper surface of the semiconductor substrate comprises an active region and an isolation region laterally adjacent to each other. A photoresist layer is patterned on top of the implant dielectric to expose regions of the implant dielectric over the active region. Nitrogen is then implanted into the active region through the implant dielectric. Nitrogen is preferably introduced into semiconductor substrate in an approximate atomic concentration of 0.5 to 2.0 percent. After the nitrogen has been implanted into a semiconductor substrate, the photoresist layer is stripped and the implant dielectric is removed. The wafer is then thermally oxidized such that a field oxide having a first thickness is grown over the isolation region and a thin oxide having a second thickness is grown over the active region. The presence of the nitrogen within the semiconductor substrate retards the oxidation rate of the silicon in the active region such that the thickness of the thin oxide is substantially less than the thickness of the thermal oxide. In a presently preferred embodiment, the field oxide has a thickness of 2,000 to 8,000 angstroms while the thin oxide has a thickness of less than 300 angstroms.

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TITLE: REDUCED BIRD'S BEAK FIELD OXIDATION PROCESS USING NITROGEN IMPLANTED INTO ACTIVE REGION

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to semiconductor fabrication and more particularly to an improved method for forming a field oxidation isolation structure by implanting nitrogen into the active regions.

2. Description of the Relevant Art

The fabrication of an integrated circuit involves placing numerous devices in a single semiconductor substrate. Select devices are interconnected by a conductor which extends over a dielectric which separates or "isolates" those devices. Implementing an electrical path across a monolithic integrated circuit thereby involves selectively connecting isolated devices. When fabricating integrated circuits it must therefore be possible to isolate devices built into the substrate from one another. From this perspective, isolation technology is one of the critical aspects of fabricating a functional integrated circuit.

A popular isolation technology used for an MOS integrated circuit involves the process of locally oxidizing silicon. Local oxidation of silicon, or LOCOS process involves oxidizing field regions between devices. The oxide grown in field regions are termed field oxide, wherein field oxide is grown during the initial stages of integrated circuit fabrication, before source and drain implants are placed in device areas or active areas. By growing a thick field oxide in field regions pre-implanted with a channel-stop dopant, LOCOS processing serves to prevent the establishment of parasitic channels in the field regions.

A conventional LOCOS process is shown in Figs. 1-6. In Fig. 1, a thin oxide 12 is grown on a semiconductor substrate 10. A layer of silicon nitride, shown in Fig. 2 as layer 14, is then deposited on the thin oxide 12 with a chemical vapor deposition process. Photoresist is then deposited on the silicon nitride layer 14 and patterned to obtain a patterned photoresist layer 15 shown in Fig. 2. Photoresist layer 15 is patterned to define an active region 16 and a field region 18 in semiconductor substrate 10.

After patterning photoresist layer 15, silicon nitride layer 14 and thin oxide layer 12 are removed in regions where the photoresist has been removed. Fig. 3 shows the wafer after the exposed silicon nitride layer 14 and thin oxide layer 12 have been removed and photoresist layer 15 has been stripped. In Fig. 4, the wafer is inserted into a thermal oxidation tube to grow an oxide in field region 18 of semiconductor substrate 10. This thermal oxidation is represented in Fig. 4 as number 20. As is well known, the presence of silicon nitride layer 14 over active region 16 suppresses the growth of oxide in those regions. Fig. 5 shows a partial cross section of the wafer after completion of thermal oxidation 20. A thick field oxide 22 is present in field region 18 of

semiconductor substrate 10 while a thin oxide 24 has been formed underneath silicon nitride layer 14 in active regions 16. A transition region between thick field oxide 22 and thin oxide 24 comprises the well known bird's beak 26. Bird's beak 26 extends into active region 16 by the amount d_1. Completion of the conventional field oxidation LOCOS process is accomplished by stripping the silicon nitride layer 14, removing thin oxide 24 with a wet etch process, growing a sacrificial oxide layer, and removing the sacrificial layer. The sacrificial oxide process is performed to eliminate the so called "Kooi" ribbons of silicon nitride that can form at the interface between thin oxide 24 and semiconductor substrate 10 during the field oxidation process. The sacrificial oxide layer is shown in phantom as a dashed line in Fig. 6.

While LOCOS has remained a popular isolation technology, there are several problems inherent with the conventional LOCOS process. First, a growing field oxide extends laterally as a bird's-beak structure. In many instances, the bird's-beak structure 26 can unacceptably encroach into the device active area 16.

In addition, it is well known that depositing CVD silicon nitride directly on a silicon surface results in a very high tensile stress that can exceed the critical stress for dislocation generation in silicon. This stress, which can create fabrication induced defects in the silicon substrate is believed to be caused by the termination of intrinsic stresses at the edges of the nitride film. To prevent this stress from affecting the semiconductor substrate 10, it is necessary in the LOCOS process to form the thin oxide layer 12, commonly referred to as a buffer oxide layer, thereby adding complexity and expense to the process.

Still further, the removal of silicon nitride layer 14 after formation of field oxide 22 is known by those skilled in the art of semiconductor processing to generate a large number of particles. When silicon nitride layer 14 is subjected to the high temperatures used to grow field oxide 22, a thin film forms on an upper surface of silicon nitride layer 14. The thin film is believed to comprise a composite of silicon, oxygen, and nitrogen ($Si_xO_yN_z$). Removal of this film from the upper surface of silicon nitride layer 14 requires additional processing steps. Instead of simply immersing the wafer in a hot phosphoric acid solution, as is commonly done to wet etch silicon nitride layers, a brief plasma etch must be performed to remove the $Si_xO_yN_z$ film from the upper surface of silicon nitride layer 14. In addition to undesirably removing oxide from an upper surface of field oxide 22, this plasma etch process is known to generate a large number of particles. These particles can become lodged on the silicon surface that can result in defective devices. Finally, the conventional LOCOS process requires a sacrificial oxide to remove the Kooi ribbons as described above. The formation and removal of the sacrificial oxide layer adds additional processing time and expense to the conventional LOCOS process. In addition, the sacrificial oxide is generally over-etched to ensure that all traces of silicon nitride formed during the field oxidation process are removed. The over-etch undesirably reduces the thickness of the field oxide 22.

Therefore, it would be highly desirable to implement a field oxidation process sequence which eliminated the need to deposit a silicon nitride layer on the wafer surface. By eliminating the nitride deposition step, such a process w uld thereby eliminate the high particle counts associated with the nitride strip process and would eliminate the field oxide etch back cycle required in conventional field oxidation process sequences.

Further, the elimination of the nitride deposition from the field oxidation process would eliminate the need to grow the Kooi oxide after removal of the nitride layer. In addition, the bird's beak structure and the encroachment problems associated with conventional field oxidation processes would be substantially reduced.

SUMMARY OF THE INVENTION

The problems identified above are in large part resolved by a semiconductor process in which field oxidation is accomplished without the use of the silicon nitride layer. The improved process hereof incorporates nitrogen into the silicon substrate instead of placing a layer of nitride on an oxide layer above the silicon substrate. The nitrogen is placed in the active region of the silicon substrate prior to the formation of the field oxide. The presence of nitrogen in selected regions of the silicon substrate serves to reduce the oxidation rate of the silicon in those regions. Thus, during the formation of the field oxide, the oxidation rate in the "nitrogenated" regions of the silicon substrate is less than the oxidation rate in regions lacking nitrogen. The higher oxidation rate in the non-nitrogenated regions results in a sharply delineated field oxide structure in which the bird's beak is substantially eliminated.

Broadly speaking, the present invention comprises a method of forming a self-aligned field oxide. A dielectric is formed on an upper surface of a semiconductor substrate comprising an active region and an isolation region. A photoresist layer is patterned on the dielectric layer to expose regions of the dielectric layer over active regions of the silicon substrate. Nitrogen is then implanted into the active regions of the silicon substrate through the exposed dielectric layer. The photoresist is then stripped and the dielectric layer removed from the wafer. In a presently preferred embodiment, the dielectric layer is comprised of a thermal oxide and removal of the dielectric layer is accomplished with a wet etch process. Next, the wafer is subjected to a thermal oxidation process whereby a field oxide grows over the isolation regions of the silicon substrate and a thin oxide grows over the active regions due to the lower oxidation rate of the nitrogenated silicon.

In a presently preferred embodiment, nitrogen is present in the active regions of the semiconductor substrate in an atomic percentage of approximately 0.5 to 2.0 percent. Preferably, nitrogen is implanted into the semiconductor substrate using a nitrogen dose of approximately 5×10^{13} to 5×10^{16} ions/cm^2. The field oxidation is preferably accomplished at a temperature of 900 to 1150°C to achieve a field oxide thickness of approximately 2,000 to 8,000 angstroms. A channel stop implant can be performed before or after formation of the field oxide. In CMOS processes, separate channel stop implants can be performed for each well.

The present invention further contemplates a method for forming a self-aligned field oxide wherein the field oxide has a transition region that encroaches upon the active area by a distance of less than 0.05 microns.

The present invention still further contemplates a semiconductor substrate comprising an active region and an isolation region. The active region contains approximately 0.5 to 2.0 percent nitrogen and the isolation

region, which is laterally adjacent to the active region, comprises a thermal oxide formed on the semiconductor substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and advantages of the invention will become apparent upon reading the following detailed description and upon reference to the accompanying drawings in which:

Fig. 1 is a partial cross-sectional view of a semiconductor substrate upon which a thin oxide has been grown;

Fig. 2 is a processing step subsequent to that shown in Fig. 1, in which a silicon nitride layer has been formed on the thin oxide layer and a photoresist layer has been patterned on top of the silicon nitride layer to define active regions and isolation regions;

Fig. 3 is a processing step subsequent to that shown in Fig. 2, in which the silicon nitride layer and the thin oxide layer over the isolation region have been etched and the photoresist layer has been stripped;

Fig. 4 is a processing step subsequent to that shown in Fig. 3, in which the wafer is subjected to a thermal oxidation step;

Fig. 5 is a processing step subsequent to that shown in Fig. 4 depicting the field oxide and thin oxide formed in the thermal oxidation step;

Fig. 6 is a processing step subsequent to that shown in Fig. 5 in which the silicon nitride layer has been stripped and the thin oxide removed;

Fig. 7 is a partial cross-sectional view of a semiconductor wafer upon which a dielectric has been formed;

Fig. 8 is a processing step subsequent to that shown in Fig. 7 in which a photoresist layer has been patterned onto the dielectric layer to define an active region and an isolation region;

Fig. 9 is a processing step subsequent to Fig. 8 in which nitrogen has been implanted into the silicon substrate within the active region bound by the patterned photoresist;

Fig. 10 is a processing step subsequent to Fig. 9 in which the dielectric layer and the photoresist layer have been removed and the wafer subjected to a thermal oxidation;

Fig. 11 is a partial cross-sectional view of the wafer after c mpletion of the thermal oxidation structure of Fig. 10; and

Fig. 12 is a processing step subsequent to Fig. 11 in which the thin oxide over the active region has been removed.

While the invention is susceptible to various modifications and alternative forms, specific embodiments whereof are shown by way of example and the drawing and will herein be described in detail. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the present invention as defined by the appended claims.

DETAILED DESCRIPTION OF THE DRAWINGS

Turning now to Figs. 7-12, an improved process sequence for forming a field oxide isolation structure is shown. Turning briefly to Fig. 12, isolation structure 99 is shown. Isolation structure 116 comprises an isolation region 106 within semiconductor substrate 100. Active region 108 includes nitrogen 112 incorporated into semiconductor substrate 100. In a presently preferred embodiment, nitrogen 112 is present in an atomic percentage of approximately 0.5 to 2.0 percent. Isolation region 106 is laterally adjacent to active region 108 and comprises a field oxide grown to form structure 116. Field oxide structure 116 comprises a sidewall 120 which extends substantially perpendicularly from an upper surface of semiconductor substrate 100. Substantially perpendicular sidewall 120 ensures that field oxide 116 encroaches upon active region 108 by a distance less than or equal to d_2, which is shown in Fig. 11. In a presently preferred embodiment, d_2 is approximately 0.05 microns or less.

Returning now to Fig. 7, a partial cross-section view of a semiconductor substrate 100 is shown. Dielectric 102 is formed upon the semiconductor substrate 100. Dielectric 102 is suitably comprised of a deposited or grown oxide having a thickness from 50 to 500 angstroms. Referring to Fig. 8, photoresist layer 104 is patterned on dielectric layer 102. Photoresist layer 104 is patterned such that the region of dielectric layer 102 above field region 108 of semiconductor substrate 100 is exposed. Depositing and patterning of photoresist layer 104 is preferably accomplished with photolithography steps well known in the art of semiconductor processing. After patterning of photoresist layer 104 is completed, nitrogen is implanted into active region 108 of semiconductor substrate 100 as shown in Fig. 9. In Fig. 9, the implanting of nitrogen is represented by arrows 110 while the implanted nitrogen within semiconductor substrate 100 is represented by the "X's" 112.

Fig. 10 shows a processing step subsequent to Fig. 9 after dielectric layer 102 and photoresist layer 104 have been removed and the wafer inserted into a thermal oxidation tube. The thermal oxidation is represented in Fig. 10 by wavy lines 114. The introduction of low levels of nitrogen into a silicon substrate is believed to retard the rate at which the silicon oxidizes. Accordingly, oxidation of semiconductor substrate occurs at a greater rate in isolation region 106, which is absent implanted nitrogen 112, than in active region 108. In a presently preferred embodiment, thermal oxidation 114 is formed at a temperature of 900 to 1150°C and can be performed in either an O_2 (dry) or H_2O (wet) ambient. Fig. 11 shows a partial cross section of the semiconductor substrate after completion of thermal oxidation 114. Field oxide 116, having a first thickness t_1 has been formed over isolation region 106 while thin oxide 118 having a second thickness t_2 is formed over active region 108. The oxidation rate in the nitrogenated region of semiconductor substrate 100 is believed to correspond to the amount of nitrogen present in semiconductor substrate 100. Thus, controlling the dosage of nitrogen implant 110 controls the oxidation rate of the silicon within active region 108 and thus controls the final thickness t_2 of thin oxide 118. In a presently preferred embodiment, thickness t_2 of thin oxide 118 is less than 300 angstroms while the thickness t_1 of field oxide 116 is 2,000-8,000 angstroms.

The use of nitrogen implant 110 to control the oxidation rate of silicon substrate 100 within active region 108 is also believed to substantially eliminate formation of the bird's beak structure routinely encountered in conventional LOCOS processing using silicon nitride. It is believed that the present method is capable of growing a field dielectric structure 116 adjacent to an active region 108 wherein a sidewall 120 of the field structure 116 is substantially perpendicular to an upper surface of semiconductor substrate 100. Thus, the distance d_2, which represents the amount by which field oxide 116 encroaches upon active region 108, is minimized. In the presently preferred embodiment, the encroachment d_2 is less than or equal to 0.05 microns. Returning now to Fig. 12, the isolation structure 116 is shown after removal of thin oxide 118 from the upper surface of semiconductor substrate 100. In addition to enabling differential oxidation rates within semiconductor substrate 100, the presence of nitrogen species 112 within semiconductor substrate 100 is believed to provide a barrier layer for fast diffusers such as boron and sodium. Further, the presence of nitrogen species 112 is believed to enhance the quality of the process gate oxide producing higher strength bonds with subsequently formed oxides. A channel stop implant (not shown) can be performed before or after formation of the structure shown in Fig. 12. Using commercially available MeV implanters, channel stop implants may be done post-field oxidation. In CMOS processes, separate channel stop implants can be performed on each well.

As will be obvious to one skilled in the art having the benefit of this disclosure, the process sequence depicted in Figs. 7-12 is capable of producing an isolation structure within a semiconductor substrate. It will be further appreciated that the isolation structure of the present invention substantially eliminates encroachment due to bird's beak formation. It will be still further appreciated that by eliminating deposition of a silicon nitride layer from the isolation process, the process sequence is simplified.

It is to be understood that the form of the invention shown and described in the detailed description and the drawings is to be taken merely as presently preferred examples of how a field oxide isolation structure can be formed without silicon nitride and without substantial encroachment due to bird's beak formation. Obvious variations of the method disclosed would be apparent to those skilled in the art having the benefit of this disclosure. For example, thin oxide 118 shown in Fig. 11 could be removed with a wet or dry etch process. As another example, photoresist layer 104 in Figs. 8 and 9 is used to mask the nitrogen implant 110 whereas other suitable materials may be used to form this masking function including polysilicon, for example. It is intended that following claims be interpreted broadly to embrace all these variations of the preferred embodiments disclosed.

WHAT IS CLAIMED IS:

1. A method of forming a self-aligned field oxide comprising:

forming a implant dielectric on an upper surface of a semiconductor substrate, said upper surface of said semiconductor substrate comprising an active region and an isolation region;

patterning a photoresist layer to expose regions of said implant oxide over said active region;

implanting nitrogen into said active region of said upper surface of said semiconductor substrate;

stripping said photoresist;

removing said implant dielectric layer; and

thermally oxidizing said upper surface of said substrate whereby a field oxide having a first thickness is grown over said isolation region and a thin oxide having a second thickness is grown over said active region, wherein said first thickness is greater than said second thickness.

2. The method of claim 1 wherein said implant dielectric layer comprises a thermal oxide.

3. The method of claim 2 wherein said thermal oxide is approximately 50 to 500 angstroms in thickness.

4. The method of claim 1 wherein said nitrogen is present in said semiconductor substrate in an atomic percentage of approximately 0.5 to 2.0 percent within a thickness less than 200 angstroms of a surface of said semiconductor substrate.

5. The method of claim 1 wherein the step of implanting said nitrogen is performed with a nitrogen dose of approximately 5×10^{13} to 5×10^{16} ions/cm^2.

6. The method of claim 1 wherein the step of thermally oxidizing said upper surface of said semiconductor substrate comprises is performed at a temperature of approximately 800-1150° C.

7. The method of claim 6 wherein the step of thermally oxidizing said upper surface of said semiconductor substrate is accomplished in an O_2 (dry) ambient.

8. The method of claim 6 wherein the step of thermally oxidizing said upper surface of said semiconductor substrate is accomplished in a H_2O (wet) ambient.

9. The method of claim 1 wherein said thickness of said field oxide is approximately 2000 to 8000 angstroms.

10. The method of claim 9 wherein said thickness of said thin oxide is less than 300 angstroms.

11. The method of claim 1 wherein a transition region from said field oxide to said thin oxide encroaches upon said active area by a distance less than 0.05 microns.

12. The method of claim 1 further comprising implanting a channel stop dopant into said semiconductor substrate.

13. A semiconductor device having a self-aligned field oxide formed with the process of claim 1.

14. A semiconductor substrate comprising:

an active region within a semiconductor substrate, wherein said active region contains approximately 0.5 to 2.0 percent nitrogen within a thickness less than 200 angstroms of a surface of said semiconductor substrate; and

an isolation region within said semiconductor substrate, laterally adjacent to said active region, wherein said isolation region comprises a thermal oxide formed on said semiconductor substrate.

15. The semiconductor substrate of claim 14 wherein said thermal oxide has a thickness of approximately 2000 to 8000 angstroms and further wherein said thermal oxide includes a sidewall, proximal to said active region, extending substantially perpendicularly from an upper surface of said semiconductor substrate.

16. The semiconductor substrate of claim 14 wherein said thermal oxide encroaches upon said active region by a distance less than 0.05 microns.

FIG. 1
(Prior Art)

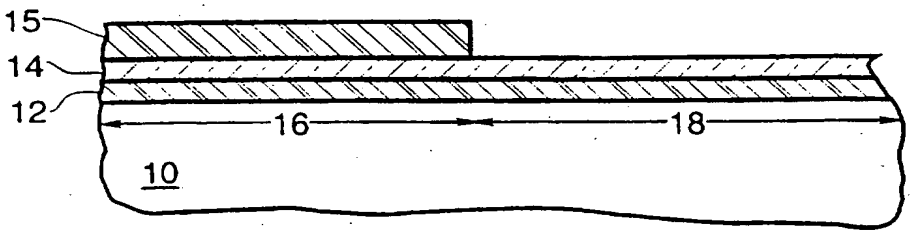

FIG. 2
(Prior Art)

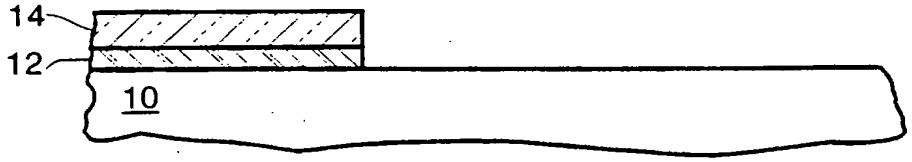

FIG. 3
(Prior Art)

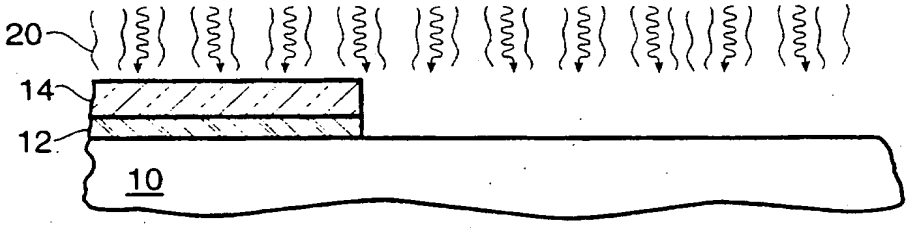

FIG. 4
(Prior Art)

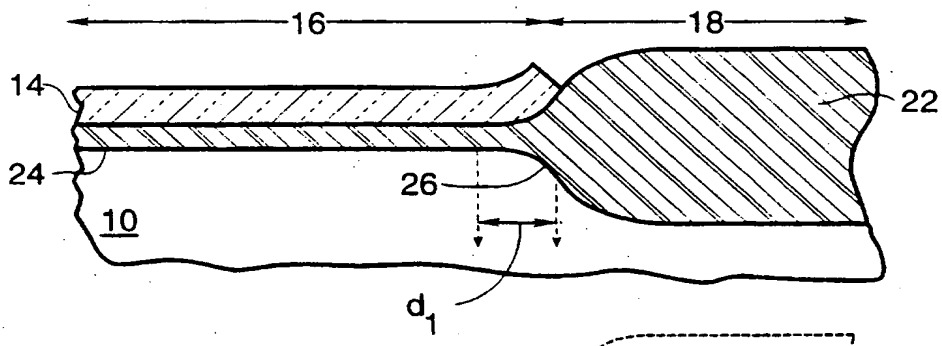

FIG. 5
(Prior Art)

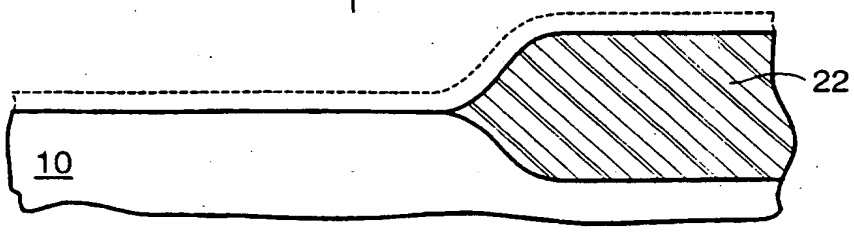

FIG. 6
(Prior Art)

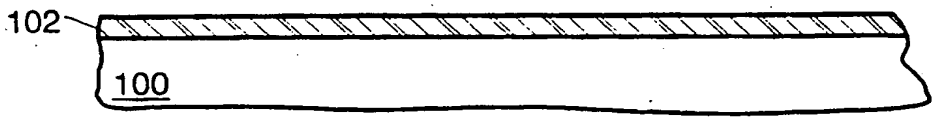

FIG. 7

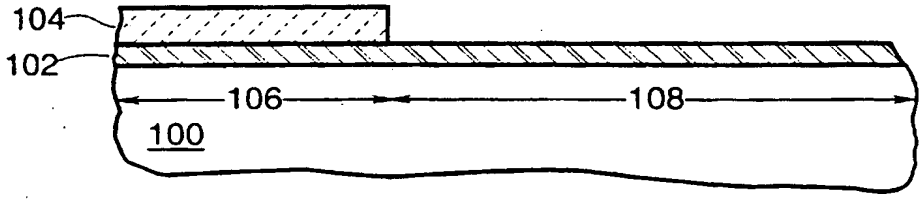

FIG. 8

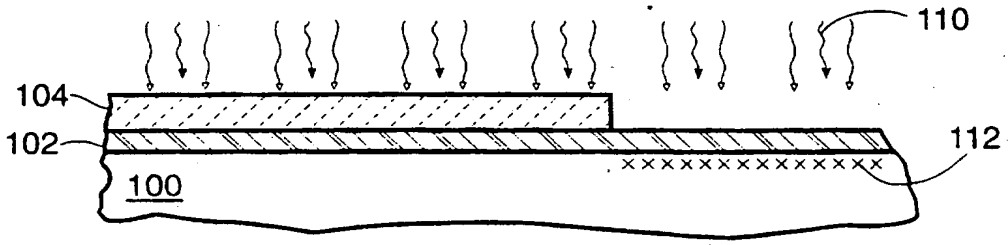

FIG. 9

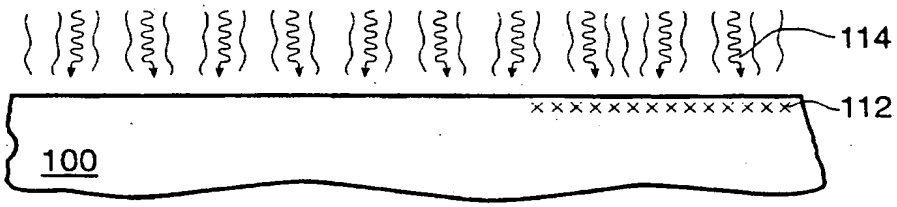

FIG. 10

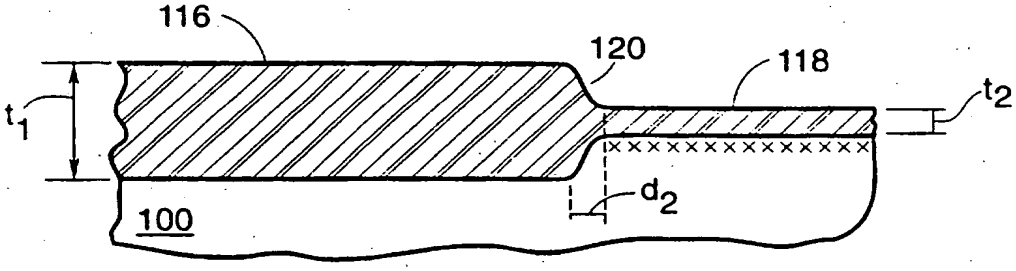

FIG. 11

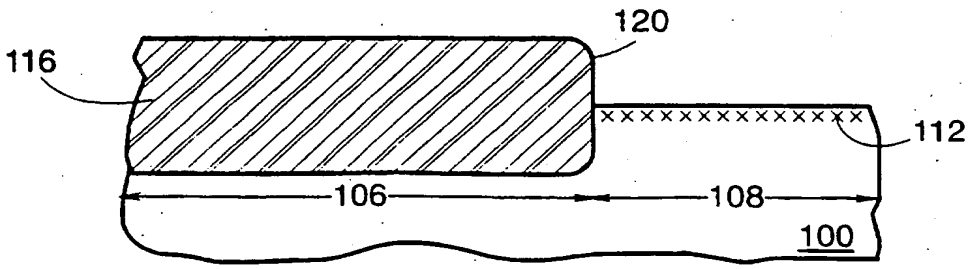

FIG. 12

INTERNATIONAL SEARCH REPORT

[redacted]ial Application No
PCT/US 97/03823

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L21/32 H01L21/762 H01L21/225

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 330 920 A (SOLEIMANI HAMID R ET AL) 19 July 1994 see column 2, line 37 - line 27; figures 1-6 ---	1,2,4-8
A	NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH, SECTION - B: BEAM INTERACTIONS WITH MATERIALS AND ATOMS, vol. B55, no. 1 / 04, 2 April 1991, pages 860-865, XP000230741 MOLLE P ET AL: "NITROGEN IMPLANTATION FOR LOCAL OXIDATION (NILO) OF SILICON" see page 860, paragraph 3; figure 1 ---	1-6,8,13
A	US 4 098 618 A (CROWDER BILLY LEE ET AL) 4 July 1978 see column 3 - column 58; figures 2A-2D ---	1,2,5, 7-9

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
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Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax (+ 31-70) 340-3016	Authorized officer Hammel, E

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